IN THE CLAIMS

1. (Original) A processor, comprising:

a plurality of registers;

circuitry configured to process a plurality of instructions associated with an instruction set including a plurality of branch and non-branch instructions, the plurality of instructions each having a multi-byte length, the plurality of instructions accessible at multi-byte aligned addresses;

wherein substantially all multi-byte aligned branch instructions are operable to access the instructions at byte aligned addresses.

2. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at word aligned addresses.

3. (Original) The processor of claim 1, wherein the plurality of instructions are accessed at half-word aligned addresses.

4. (Original) The processor of claim 1, wherein accessing the instructions comprises reading and writing the addresses.

5. (Original) The processor of claim 1, wherein branch instructions comprise branch and conditional branch instructions.

6. (Original) The processor of claim 1, wherein branch instructions comprise a branch offset and a current program counter value.

7. (Currently Amended) The processor of claim 1, wherein the units of ~~the~~ branch offset and ~~the~~ current program counter are in bytes.

8. (Original) The processor of claim 1, wherein the plurality of instructions are one word in length.

9. (Original) The processor of claim 1, wherein the branch instruction and a plurality of non-branch instructions supported by the processor are implemented using common subcircuitry.

10. (Original) The processor of claim 9, wherein common subcircuitry is used to handle the immediate field associated with the branch and non-branch instructions.

11. (Original) The processor of claim 10, wherein common subcircuitry is used to perform sign-extensions of the immediate field associated with the branch and non-branch instructions.

12. (Original) The processor of claim 1, wherein the processor is a processor core on a programmable chip.

13. (Original) The processor of claim 1, wherein the processor is a processor core on a ASIC.

14. (Original) A processor, comprising:

a plurality of registers;

circuitry configured to process a plurality of branch and non-branch instructions associated with an instruction set, the plurality of branch instructions and non-branch instructions including an immediate field;

wherein common subcircuitry is used to process the immediate field associated with one or more branch instructions and one or more non-branch instructions.

15. (Original) The processor of claim 14, wherein the instruction set comprises a plurality of instructions.

16. (Original) The processor of claim 15, wherein the plurality of instructions are accessed at half-word aligned addresses.

17. (Original) The processor of claim 14, wherein branch instructions comprise branch and conditional branch instructions.

18. (Original) The processor of claim 14, wherein common subcircuitry is used to handle the immediate field associated with the branch and non-branch instructions.

19. (Original) The processor of claim 18, wherein common subcircuitry is used to perform sign-extensions of the immediate field associated with the branch and non-branch instructions.

20. (Original) A method for performing an instruction, the method comprising:

decoding a branch instruction associated with an address, the branch instruction having an associated opcode and an immediate value;

calculating a branch target address using the immediate value, wherein the branch target address is determined by using common subcircuitry, the common subcircuitry operable to calculate a byte-aligned address, wherein the common subcircuitry is also configured to perform nonbranch operations;

jumping to the branch target address, wherein the branch target address is multi-byte aligned.

21. (Currently Amended) The method of claim 20, wherein the branch target address is word ~~multi-byte~~ aligned.

22. (Original) The method of claim 20, wherein the branch target address is half-word aligned.

23. (Original) The method of claim 20, wherein calculating the branch target address comprises performing a sign extend operation.

24. (Original) The method of claim 20, wherein the branch instruction calculates the branch target address using the immediate value and the address of the branch instruction.

25. (Original) The method of claim 20, wherein the units of the immediate value and the address associated with the branch instruction are in bytes.

26. (Original) The method of claim 25, wherein the address associated with the branch instruction is a program counter.

27. (Original) A processor, comprising:

means for decoding a branch instruction associated with an address, the branch instruction having an associated opcode and an immediate value;

means for calculating a branch target address using the immediate value, wherein the branch target address is determined by using common subcircuitry, the common subcircuitry operable to calculate a byte-aligned address, wherein the common subcircuitry is also configured to perform nonbranch operations;

means for jumping to the branch target address, wherein the branch target address is multi-byte aligned.

28. (Original) The processor of claim 27, wherein the branch target address is multi-byte aligned.

29. (Original) The processor of claim 27, wherein the branch target address is half-word aligned.

30. (Original) The processor of claim 27 included in a programmable chip.